CLAIMS:

1. A testing unit (10) for testing a device under test – DUT – (30), comprising:

a signal generator (20) adapted for applying a stimulus signal to the DUT (30),

a receiving unit (50) adapted for receiving a response signal from the DUT on the applied stimulus signal, and

a synchronizing unit (40) for synchronizing a data flow of the response signal between the DUT (30) and the receiving unit (50), whereby the synchronizing unit (40) receives a first clock signal (DUT-CLK) from the DUT (30) and a second clock signal (CLK) of the testing unit (10), the synchronizing unit (40) comprising:

a buffer (70) for buffering data,

a write unit (80) for writing data from the DUT (30) into the buffer (70), whereby a write access onto the buffer (70) is controlled by the first clock signal (DUT-CLK),

a read unit (90) for reading out data from the buffer (70) to be provided to the receiving unit (50), whereby a read access onto the buffer (70) is controlled by the second clock signal (CLK).

2. The testing unit (10) of claim 1, wherein the buffer (70) comprises a register structure (70) with a plurality of registers (70A-70H).

3. The testing unit (10) of claim 2, further comprising:

a write pointer (100) adapted to be moved between the pluralities of registers (70A-70H) for defining one of the plurality of registers (70A-70H) to receive and buffer data from the DUT (30), and

a read pointer (110) adapted to be moved between the plurality of

registers (70A-70H) for defining one of the pluralities of registers (70A-70H) to be read out.

4. The testing unit (10) of claim 3, wherein the write pointer (100) is adapted to be clocked by the first clock signal (DUT-CLK) for successively writing successive data words from the DUT (30) to different registers (70A-70H), and the read pointer (110) is adapted to be clocked by the second clock signal (CLK) for successively reading out successive data words buffered in the plurality of registers (70A-70H).

5. The testing unit (10) of claim 1, wherein the write unit (80) comprises a latch controlled by the first clock signal (DUT-CLK), so that successive data words can be latched with the first clock signal (DUT-CLK) and thus successively written into the buffer (70).

6. The testing unit (10) of claim 1, wherein the buffer (70) is adapted to provide an initial delay time between a first valid write access and a first valid read access.

7. The testing unit (10) of claim 6, wherein the initial delay time is provided dependent on the maximum expected variation between such write and read accesses.

8. A method for testing a device under test – DUT – (30), the method comprising the steps of:

(a) applying a stimulus signal to the DUT (30),

(b) writing data in response to the stimulus signal from the DUT (30) into a buffer (70), whereby a write access onto the buffer (70) is controlled by a first clock signal (DUT-CLK) of the DUT (30),

(c) reading out data from the buffer (70) to be provided to a receiving unit (50), whereby a read access onto the buffer (70) is controlled by a second clock signal (CLK) of the receiving unit (50),

(d) receiving the read out data in response to the stimulus signal by the receiving unit (50).

9. The method of claim 8, further comprising a step of initializing a first valid write access and/or a first valid read access.